A Discussion on IGBT Short-Circuit Behavior and Fault Protection Schemes

Rahul S. Chokhawala, *Member, IEEE,* Jamie Catt, *Member, IEEE,* and Laszlo Kiraly

Abstract— **IGBT's are available with short-circuit withstand times approaching those of bipolar transistors. These IGBT's can therefore be protected by the same relatively slow-acting circuitry. The more efficient IGBT's, however, have lower short-circuit withstand times. While protection of these types of IGBT's is not difficult, it does require a reassessment of the traditional protection methods used for the bipolar transistors. An in-depth discussion on the behavior of IGBT's under different short-circuit conditions is carried out and the effects of various parameters on permissible short-circuit time are analyzed. The paper also rethinks the problem of providing short-circuit protection in relation to the special characteristics of the most efficient IGBT's. The pros and cons of some of the existing protection circuits are discussed and, based on the recommendations, a protection scheme is implemented to demonstrate that reliable short-circuit protection of these types of IGBT's can be achieved without difficulty in a PWM motor-drive application.**

I. Introduction

POWER transistors used in motor-drive application need to be protected from failure under external fault conditions. Such faults mostly result from the occurrence of a short circuit at the load end. Motor winding insulation failure, for example, may cause a fault in the system. Also there is always a threat of wiring misconnections at the motor terminals creating a possibility for the drive output terminals to be short-circuited. In the case of dedicated motor drives—where the complete systems are assembled prior to shipping—such mistakes are not nearly as likely to occur. In applications such as uninterruptible power supplies, filter chokes used in the system would limit the rate of rise of fault currents, allowing a slower overcurrent detection circuit to protect the system. In high-frequency welding power supplies, an application where IGBT's are becoming the favored devices, excessively high fault currents are prevented by the resonant nature of the power circuit and/or output transformer leakage inductance.

The switching devices are selected by system designers to reliably handle circuit currents under normal, as well as estimated overload, conditions. Under fault conditions, however, a device could be subjected to very high surge currents, with magnitude limited mainly by its own gain. Only timely control and removal of the fault current by some external means would save the switching device from failure. In applications where a system fault is a possibility, external protection circuits are used to sense the fault and turn off the transistors by shutting down the base/gate drive. In all such applications, except where "intelligent" modules are used, the protection circuit is connected externally to these devices.

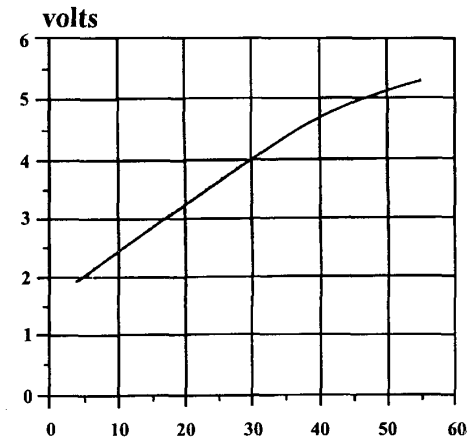

Fig. 1. $V_{CE(on)}$ versus t_{sc}. Generalized trade-off curve.

Switching device manufacturers are expected to guarantee minimum short-circuit withstand time—a measure of how long a device would survive under specified test conditions. What complicates the picture is the fundamental device trade-off between short-circuit withstand time and transistor current-gain. The higher the gain of the transistor, the higher will be the fault current magnitude and the shorter will be the short-circuit withstand time [1], [2]. The generalized trade-off plot, illustrated in Fig. 1, is most important to the IGBT manufacturers due to the inherently higher gain of their devices. The low-gain IGBT's available today allow longer short-circuit time but at the expense of operating efficiency. The high-gain devices, on the other hand, boast greater efficiency but require more "alert" protection circuits.

IGBT's available in the initial phase of their evolution were of the low-gain type with short-circuit time approaching that of BJT's. Designing-in of these devices has been, to a great part, responsible for the still-prevalent market demand for these less efficient but >10-μs-short-circuit-time IGBT's. The present trend, however, is towards high-gain, low-loss IGBT's. The purpose of this paper is to show how various circuit parameters and fault conditions affect the short-circuit endurance time of these devices and how an effective protection scheme could be

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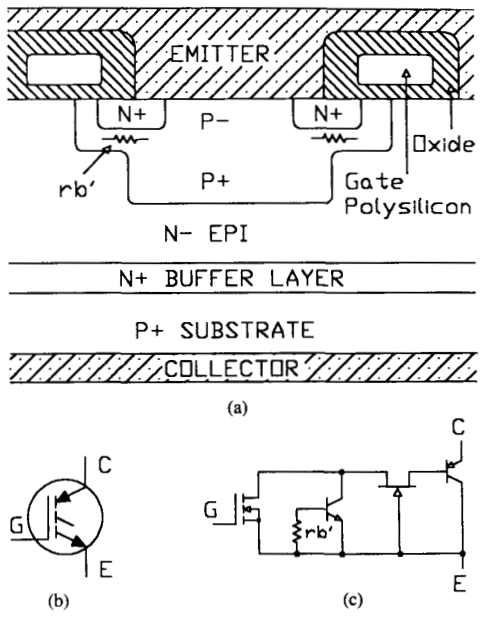


Fig. 2. (a) Silicon cross section of an IGBT, (b) with its symbol, and (c) equivalent circuit.

implemented. The intent is also to demonstrate, via a practical experiment, that such a scheme can provide full short-circuit protection, even for more efficient, high-gain IGBT's with modest intrinsic short-circuit capability.

II. The Failure Mechanisms

It can be seen from Fig. 2 that an IGBT is a four-layer structure. The structure is similar to a MOSFET except that a heavily doped p-type layer is added. A p-n-p transistor is formed with its emitter at the substrate and its collector, the p body region, connected to the top-layer metal. A parasitic n-p-n transistor is also formed with its collector in the n-type epi region and its emitter also at the top-layer metal. An equivalent circuit for the IGBT is also shown in Fig. 2. The combination of the two transistors produces a structure similar to that of a thyristor [3].

The destruction of an IGBT under short circuit is always due to an excessive power dissipation generating high temperatures beyond the limits of the silicon. The high temperatures occur in concentrated locations due to nonuniformity of the dopant concentrations. The processes leading to the breakdown of the silicon may vary depending on the failure mode of the device. Some of these processes and their failure modes are discussed below.

A. Exceeding Thermal Limit

If short circuit is sustained on a device, the power dissipation of the high current will cause a temperature rise to occur. This temperature rise in the die is extremely fast due to its fast thermal time constant. Exact calculations of the temperature rise are difficult due to the transient thermal impedance model not being accurate at the extremely high power dissipation occurring under short-circuit conditions.

The silicon will not fail immediately even if the rated junction temperature for the device is exceeded. At approximately 250°C, however, the doped silicon becomes intrinsic. Further rise in junction temperature would lead to exponential increase in the carrier concentration and result in thermal runaway [7]. The die becomes fatally damaged when the silicon begins to break down above 900°C. There also is a possibility of silicon, near its surface, reaching the metal–silicon interface eutectic temperature (577°C for Al–Si). If this takes place, contact-metal would migrate into the silicon and to the junctions, fatally harming the blocking capability of the device in the process. These temperatures are reached in such a short time, after the die becomes intrinsic, that it is not possible to save the device by external means.

B. Latching

As described earlier, the four-layer structure of the IGBT resembles that of a thyristor. The thyristor is prevented from operating by limiting the gain of the two transistors and reducing the value of the parasitic resistor rb'.

Under fault conditions excess current can flow through rb' as the MOSFET channel is reduced when attempting to turn off the IGBT. This excess current can cause a voltage across rb' that drives part of the IGBT structure into a latch condition. Once this occurs, control of the IGBT from the gate is not possible. An extremely low impedance is presented across the IGBT which was supporting the supply voltage. The high current, limited only by the supply impedance, and high-power dissipation quickly destroys the device. Thus an IGBT rated for long short-circuit time may fail at the turn-off simply due to the "dynamic latching." Since the turn-off speed is to some degree dependent on the turn-off gate resistors, IGBT manufacturers must specify their values along with other test conditions.

C. Exceeding Voltage Rating

An IGBT may survive long short-circuit time but fail when turned off. The fall rate of current induces a voltage equal to $L \cdot di/dt$ in the circuit stray inductances. This voltage overshoot, if too large, would cause the switching device to avalanche, resulting in failure due to excessive power surge or latching.

This mode of failure could be avoided by minimizing the circuit stray inductances on the dc side of the switching device, also called "dc loop" inductance (see Fig. 5). The objective could also be achieved by slowing the rate of fall of fault current, which again to some degree is dependent on the turn-off series gate resistor, $R_{G(\text{off})}$. The higher the value of $R_{G(\text{off})}$, the slower is the current rate of fall. The above is a subject of discussion in a later section.

III. Reliability

Short circuit is a fault condition that will drive the operation of the IGBT outside its safe operating area. A short-circuit protection scheme, while saving a device from immediate failure, may not stop the long-term reliability of the device

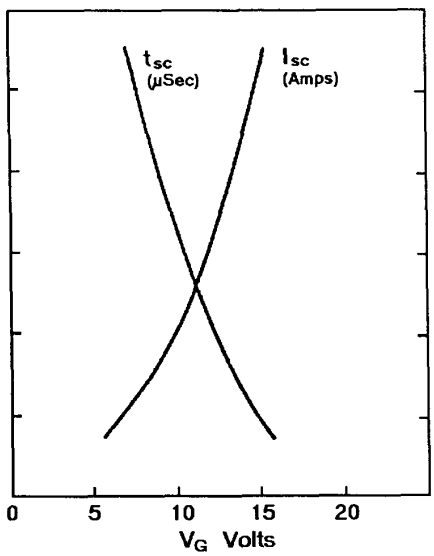


Fig. 3. Generalized trends of short-circuit current, I_{sc}, and permissible short-circuit time, t_{sc}, with gate voltage V_G.

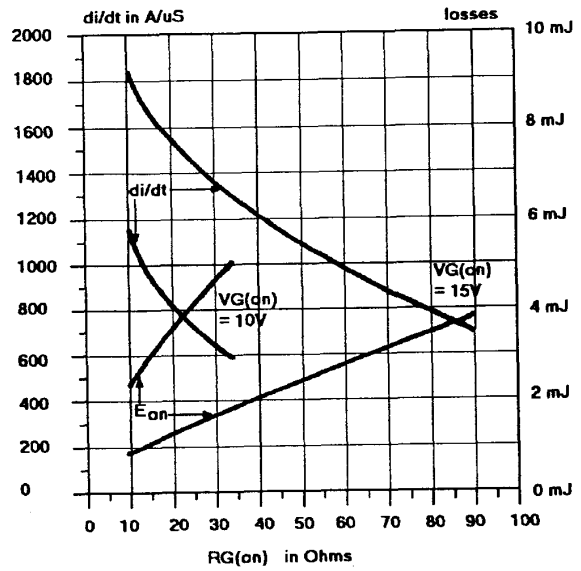


Fig. 4. Turn-on di/dt and losses versus $R_{G(on)}$. IRGTA090F06 tested at 360 V, 50 A, 150°C. L_S = 100 nH.

from being affected. Care needs to be taken in specifying the short-circuit capability of a device until the long-term reliability effects are better known. For this reason the designer should limit the short-circuit stress the IGBT is subjected to in an effort to reduce any detrimental effects on the reliability of a device. An effort should be made to immediately remove the IGBT fault current, once the existence of fault condition is confirmed. It is thus advisable to protect a 10-μs-short-circuit-time IGBT in, say, 2 μs.

IV. IGBT Short-Circuit Behavior

The ability of an IGBT to withstand fault currents can be improved by reducing the gate voltage applied to the device. A general trend in variation of short-circuit current I_{sc}, and time t_{sc}, with gate-drive voltage is illustrated in Fig. 3. Reducing gate voltage to an IGBT reduces the magnitude of fault current through it and as a result extends the short-circuit time.

In Fig. 4, turn-on losses are plotted against gate-drive voltage for two values of series gate resistors. It can be seen that within certain limits, "high" gate-drive voltage and "high" gate resistance will produce the same current rise time and turn-on energy dissipation as "low" gate-drive voltage and "low" gate resistance. Thus for the device considered, identical turn-on waveforms could be obtained with a $V_{G(on)}R_{G(on)}$ combination of 15 V–50 Ω as with 10 V–10 Ω. This is only true, however, as long as the gate-drive voltage is high enough to support the peak turn-on current [4]. Note that the turn-off switching losses are not an issue here since they are largely unaffected by the gate drive.

A. Types of Fault

Two types of fault conditions are possible. The behavior of IGBT's and the relationship to the gate-drive circuitry should be understood for each case.

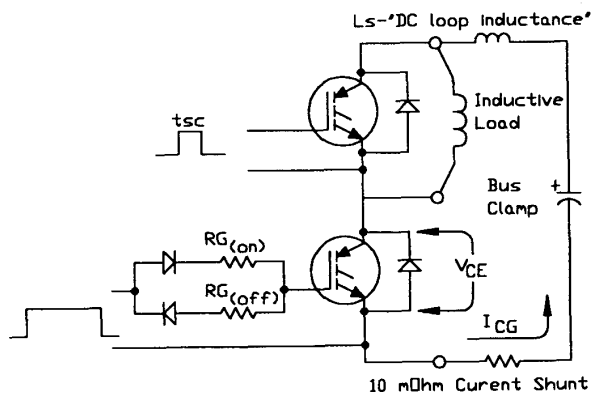


Fig. 5. Short-circuit test circuit.

1) Fault under Load: A device may be subjected to a short circuit while in normal conduction. The test circuit is shown in Fig. 5. The waveforms in Fig. 6 illustrate this type of fault. Initially the IGBT is gated on and is operating normally, carrying a steady load current within its ratings (= 80 A). The voltage across the device, v_{CE}, is low. A fault is imposed on the device by turning the complementary IGBT shown in Fig. 5 on, causing a shoot-through. The current increases rapidly, pulling the IGBT out of its near saturation state. The rise in the v_{CE} causes a current i_{CG} to flow through the Miller capacitance, C_{CG}. Due to the presence of a high $R_{G(off)}$ (= 100 Ω), the gate-emitter voltage jumps to a higher level (from 11 V to 17 V). Consequently, the fault current, for this high-gain IGBT, rises to over 1200 A before declining as v_{GE} dwindles back to its normal on-state value. The fault current in this experiment was removed by turning the complementary IGBT switch off.

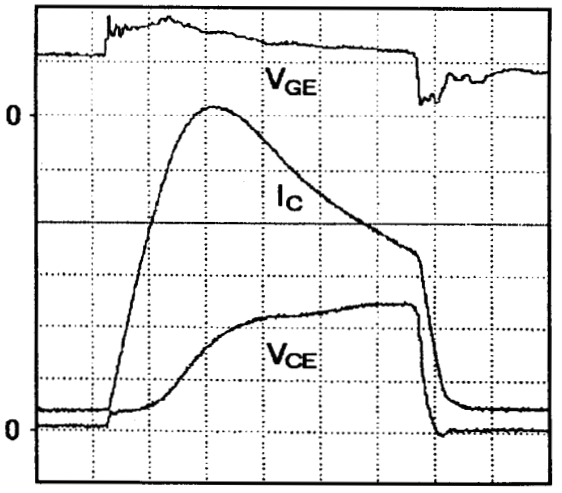


Fig. 6. Fault under load test waveforms—IRGTA090F06 tested at 360 V, $V_{G(\text{on-state})}$ = 11.0 V, $R_{G(\text{on})}$, $R_{G(\text{off})}$ = 100 Ω. V_{CE}: 100 V/div, I_{C}: 200 A/div, V_{GE}: 10 V/div, time: 500 nS/div.

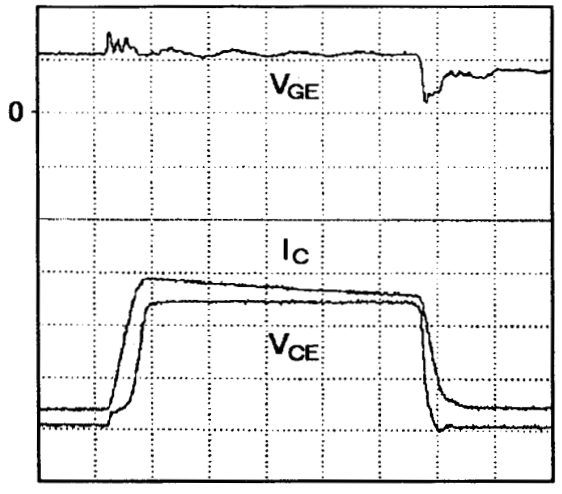


Fig. 7. Fault under load test waveforms—IRGTA090F06 360 V, $V_{G(\text{on-state})}$ = 11.0 V, $R_{G(\text{on})}$ = 100 Ω, $R_{G(\text{off})}$ = 10 Ω. V_{CE}: 100 V/div, I_{C}: 200 A/div, V_{GE}: 10 V/div, time: 500 nS/div.

Lowering the value of $R_{G(\text{off})}$ facilitates better clamping of the gate-emitter voltage, thereby significantly reducing the fault current magnitude. As demonstrated in Fig. 7, the fault current peak decreases to less than 600 A when $R_{G(\text{off})}$ is reduced to 10 Ω.

An increase in V_G would result in an increase in the fault current magnitude. The IGBT has a better chance of survival with lower fault current level and hence lower resulting power dissipation. The short-circuit endurance time is increased, allowing the protection circuits longer time to react. IGBT's designed for higher operating efficiency, due to inherently higher gain, have less short-circuit endurance time than less efficient devices.

2) Hard Switch Fault: The inductive load in Fig. 5 is short-circuited and the switching device is gated on, directly into the fault. In this mode the IGBT is off and the system voltage is supported across the device. The rate at which the device begins to conduct current and the magnitude of the fault current are related to the charging rate of the input capacitance and the gate-drive voltage V_G. This type of fault is described by the waveforms in Fig. 8.

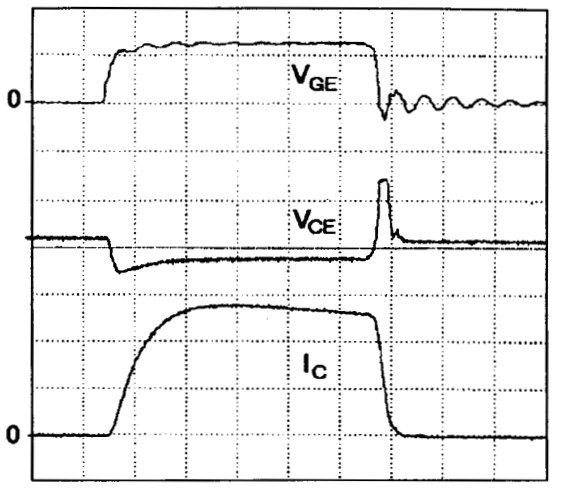


Fig. 8. Hard switch fault test waveforms—IRGTA090F06 420 V, $V_{G(\text{on-state})}$ = 12.5 V, $R_{G(\text{on})}$ = 33 Ω, $R_{G(\text{off})}$ = 0 Ω. V_{CE}: 100 V/div, I_{C}: 200/A/div, V_{GE}: 10 V/div, time: 1 μs/div.

During the prefault stage the full system voltage is supported by the device. Upon application of the gate signal and following the gate-emitter voltage reaching gate-threshold voltage, i_C begins to rise. A notch is gouged out of v_{CE} due to the voltage drops occurring across the resistive and inductive elements of the circuit.

The fault current was ended by simply removing the gate drive. The rapid fall of the fault current combined with the "dc loop" inductance causes v_{CE} to overshoot the supply voltage. In this particular case, the voltage overshoots the bus voltage by 130 V. The rate of fall of fault current and hence the magnitude of V_{CE} can be controlled to a certain degree, by varying the value of $R_{G(\text{off})}$. The device was retested with $R_{G(\text{off})}$ increased to 33 Ω. As viewed from Fig. 9, the resultant voltage overshoot decreases to 100 V.

Note that increasing $R_{G(\text{off})}$ to reduce the overvoltage transient following short circuit is in conflict with other considerations, the gate noise immunity and the dv/dt capability being the main ones, as discussed elsewhere [1]. A trade-off will have to be made by the designer, based on his specific operating conditions.

It is obvious from Figs. 8 and 9 that for a hard switch fault (HSF) only a small positive dv/dt is generated across the IGBT. Thus the Miller effect, a major consideration for the fault under load, has much less influence for the hard switch fault, particularly because the Miller capacitance is much lower at higher voltage. Thus the hard switch fault can result in much lower fault current than the fault under load. This is probably why an HSF test is used by most manufacturers to quote the short-circuit capabilities of their devices, because it is a less stressful test and will tend to give flattering results.

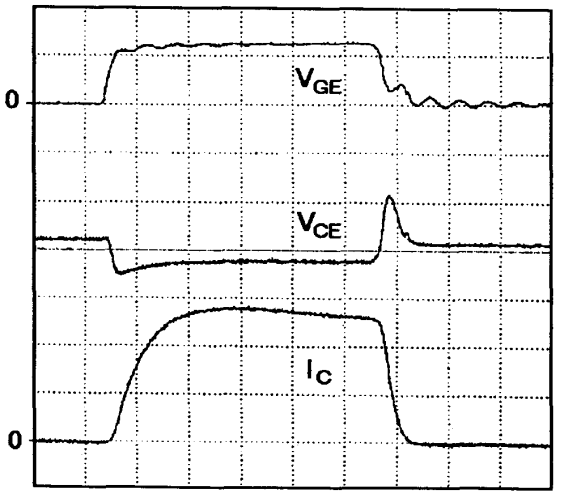


Fig. 9. Hard switch fault test waveforms—IRGTA090F06 tested at 420 V, $V_{G(\text{on-state})}$ = 12.5 V, $R_{G(\text{on})}$, $R_{G(\text{off})}$ = 33 Ω. V_{CE}: 100 V/div, I_C: 200 A/div, V_{GE}: 10 V/div, time: 1 μs/div.

B. Short-Circuit Protection Schemes

Many schemes have been discussed over the last few years for protecting IGBT's under fault conditions [5]. All of these schemes have their advantages and disadvantages. The degree to which they perform the protection function for the cost of implementation is a decision to be made by the design engineer.

The following attributes are considered desirable for a protection scheme to possess:

1) The scheme must implement a shutdown of the IGBT before device failure occurs. This should be true for all operating conditions the IGBT will be subjected to.
2) The scheme should limit the peak fault current allowed to pass through the IGBT and therefore reduce the stress on the device and other parts of the system which are exposed to the high current.
3) The scheme should be insensitive to noise and nuisance trips. Switching circuits generate noise due to high switching di/dt's and stray circuit inductances. The fault detection method should ignore this noise as well as transient overcurrents due to such things as diode recovery.
4) The scheme should be flexible enough to operate under "Fault Under Load" and "Hard Switch" type faults.
5) The scheme should not detrimentally affect the switching performance of the IGBT. This reflects on the operating efficiency of the system and the reliability of the part due to increased temperature.
6) The scheme should not detrimentally affect the conduction performance of the IGBT. This reflects on the operating efficiency of the system and the reliability of the part due to increased temperature.
7) The trip point of the scheme should be easy to set at some level that accurately defines the occurrence of a fault condition.
8) It is desirable for the scheme to be inexpensive and simple to implement so as to not affect the economic viability of an application.

The above characteristics of a protection scheme are strongly linked to the detection method used to determine the existence of a fault condition. A review of some detection methods follows and their impact on the above points is briefly summarized.

Resistor Sensing: This method of fault detection is probably the most straightforward to understand. A shunt resistor is placed in the load current path and used to generate a voltage that is monitored by the protection circuit. The advantages of using sense resistors are:

1) Accurate current measurement suitable for both overcurrent and short-circuit detection.
2) Signal may also be used for analog feedback.

The disadvantages of using sense resistors are:

1) Bulky, expensive low-inductance sensing resistor is required.
2) Bad transient response due to the self-inductance of the sense resistor and the wiring inductances. If the resistor is placed in the dc loop, it will add unwanted inductance that may affect performance of the system.
3) The voltage from the sense resistor is not isolated from the main power circuit. This means that either the protection circuit may have to be isolated from the main logic circuitry or the fault detection signals passed through an isolation barrier which adds complexity to the system.

The use of current-sensing IGBT's may involve a sensing resistor in the current sense path. This resistor can be a more convenient value than a resistor in the main current path; however, the cost trade-off of the more expensive IGBT, the limited availability, and the consistency of the sense ratio from device to device will have to be evaluated.

Current Transformer: This is another obvious method for fault current detection. A current transformer is placed around a conductor that is expected to carry any fault current and the output monitored. The advantages of using a current transformer are:

1) The transformer can be chosen to provide accurate ac sensing.
2) The transformer provides isolation between the power circuit and the protection circuit which can now be more conveniently referenced.
3) The protection circuit is current driven and can provide a high-level signal output that offers more noise immunity.

The disadvantages of using a current transformer are:

1) The current transfer system cannot easily sense dc levels unless a more sophisticated but expensive dc transformer is used. The Hall Effect sensors provide one such example.
2) The design of an appropriate current transformer is not a trivial matter as it must be able to operate over a wide bandwidth. To respond to fast-rising fault currents it must be able to operate up in the MHz region as well as down to the minimum switching frequency of the system.

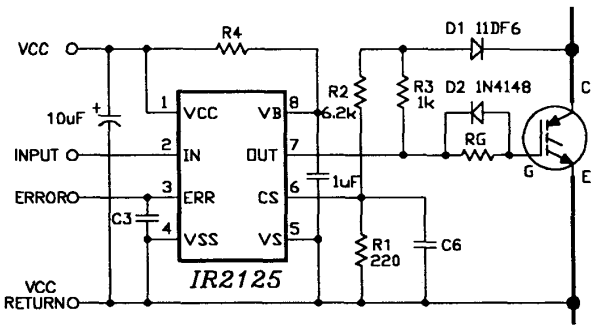


Fig. 10. IGBT gate drive and short-circuit protection scheme. V_{CE} sensing using IR2125 PIC.

V_{CE} Sensing: This scheme is also referred to as "desaturation detection" [5], [6]. By definition, short circuit means that the only impedance seen by the supply is the switching device. The supply voltage will therefore appear across the device. For this to occur the IGBT is pulled out of its low on state voltage mode and driven up the output characteristic curve. This voltage across the device when it should be in the low on state can be detected. The advantages of the V_{CE} sensing method are:

1) No lossy current sense element is required in the circuit.
2) The circuit can be fast because of the low circuit inductances.
3) The circuit will be equally effective in ac and dc applications.
4) The circuit is inexpensive and would be easy to integrate as it uses simple passive components.

The disadvantages of the V_{CE} sensing method are:

1) The circuit cannot be set to a known current level and gives a coarse fault/no-fault indication. The circuit will have to be set so that its detection level is above the maximum $V_{CE(on)}$ of the IGBT to determine when it is pulling out of saturation.
2) The circuit is not isolated from the power stage. This means that while an immediate action of removing the gate signal to the IGBT could be carried out locally, passing the error message to the logic circuitry (flagging) may require an isolation barrier, adding to the complexity of the system.
3) The circuit should provide blanking time to allow for the turn-on switching process.

C. A Practical Circuit

An inexpensive way to drive and fast-protect an IGBT is shown in Fig. 10. The circuit uses the IR2125 MOS gate-driver PIC [8]. The current sense feature of this device was modified to function as V_{CE}-sense. During normal IGBT conduction, V_{CE} is near saturation value and diode $D1$ is forward biased. The values of resistors $R1, R2$, and $R3$ are adjusted to keep the potential across $R1$—also PIC's CS pin—well below triggering value during normal operation. The IGBT gate drive remains unaffected.

When a fault occurs, say, due to accidental shorting of the load, rapid rise in V_{CE} reverse biases the diode, $D1$. The gate drive now starts to charge capacitor $C6$. The time constant $(R2 + R3)C6$ is adjusted to provide a dead time which is long enough to allow for the turn-on switching to complete, or harmless capacitive loads transients. Note that IR2125 does have a built-in dead time of 500 ns.

When the voltage at the CS pin rises above the threshold level, the protection circuit inside the PIC is triggered. The gate drive is removed after reaction time, that is partly set by the capacitor $C3$ at the error pin. The reaction time of this protection circuit is as low as 1.5 μs, which is fast enough to protect most efficient IGBT's. Detection of a fault is reported at the ERROR pin 3.

Note that the circuit in Fig. 10 is configured to drive and protect a low-side switch. IR2125 serves as both high-side (to 500 V) and low-side driver. For high-side operation, a bootstrap diode is required between V_{CC} and V_B pins. The purpose of resistor $R4$ is to decouple output stage from the input stage and help minimize IGBT switching noise feedback. Diode $D2$ provides low reverse impedance and reduces the Miller effects.

D. Short-Circuit Protection of IGBT's in a Three-Phase PWM Motor Drive

The practical application of the protection circuit shown in Fig. 10 was demonstrated using a 5-hp ac motor drive. The system was set up as shown in Fig. 11. To assure protection of the high-gain IGBT's used in this experiment, capacitor $C6$ was adjusted to react in 1.5 μs and $C3$ was adjusted to achieve total reaction time of 3 μs. The waveforms of Fig. 12(a) illustrate operation of the above protection circuit. The figure shows PWM voltage and sinusoidal motor-drive output current under blocked rotor condition. A short was forced across the motor-drive output terminals at time $t1$. This activated the protection circuit, resulting in IGBT's turning off. The IGBT fault current appears as a current spike in the inverter output current waveform. Fig. 12(b) shows the IGBT current waveform during the fault condition, on an expanded time scale. The current shot up from 32 A under blocked rotor conditions to 84 A under fault conditions. For higher gate-drive voltages, fault current would have increased. The gate to the switching device was removed, saving it from an imminent failure. The flag output at the ERROR pin tripped a logic circuit which shut down further gating of all the IGBT's. Note that by adjusting the value of the capacitor at the ERROR pin the circuit reaction time could be further reduced.

The test was repeated with the motor running under no load conditions. The inverter output current waveform shown in Fig. 13 reflects the small magnetizing motor current. The figure also shows the inverter PWM output voltage waveform. The output terminals of the inverter were momentarily shorted out at instance $t1$. Just as in the earlier case, protection circuit action turned off the IGBT's in 5 μs. The short was removed at $t2$. Thereafter, the motor current ceased to flow through the shorted path and the sinusoidal back EMF voltage appeared at the motor terminal.

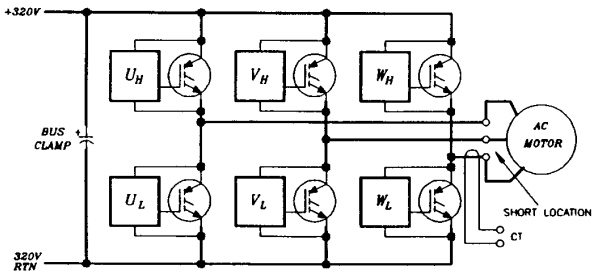
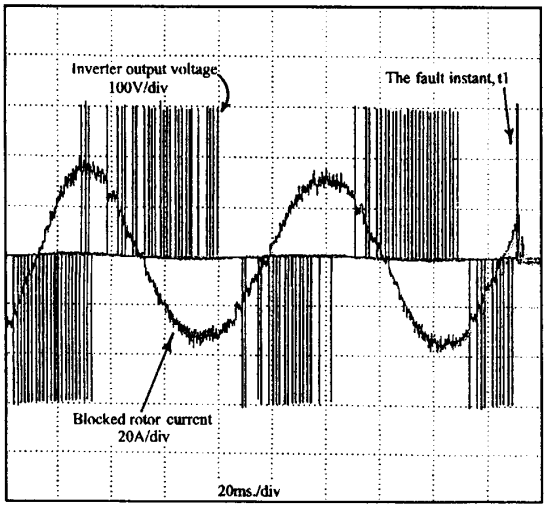
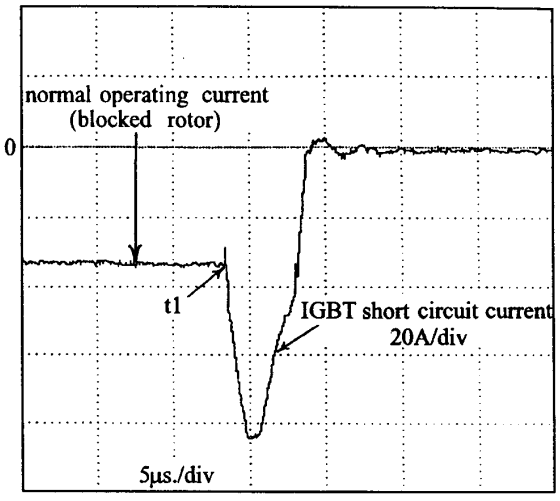


Fig. 11. IGBT PWM three-phase motor drive with V_{CE}-sensing fault protection scheme.



(a)



(b)

Fig. 12. (a) Short-circuit test under blocked rotor condition. PWM inverter output voltage and motor current. (b) IGBT current waveform.

Fig. 12(b) demonstrates the point that inexpensive circuits are available to (drive and) protect low-t_{sc} but more efficient IGBT's.

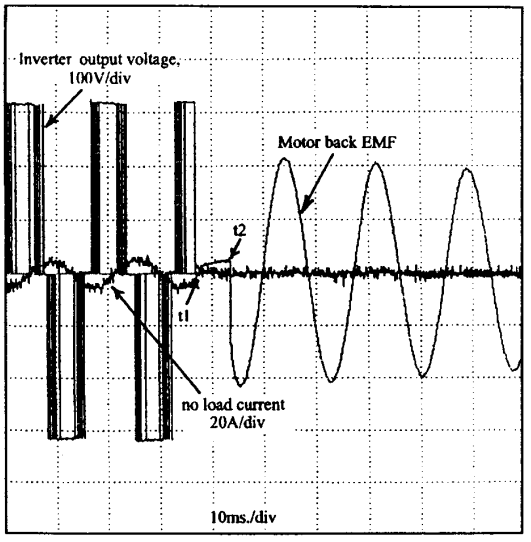


Fig. 13. Short-circuit test with the motor in free-run. PWM inverter output voltage and motor current.

V. Conclusion

The issue of short-circuit capability and protection of IGBT's is receiving a great deal of discussion in certain applications, in particular, applications such as motor drives where there is potential for the end product user to incorrectly connect up a system. The IGBT is a more efficient device than what is currently being used in these applications and as such has a lower short-circuit capability and will require faster protection circuits than those for low-gain, less-efficient BJT's.

The failure modes and mechanisms of the IGBT have been discussed in an effort to determine the important criteria for a protection circuit. Methods of fault detection have also been discussed and their general advantages and disadvantages pointed out so that an appropriate detection method may be selected for a given application. The so-called "V_{CE} detection" method appeared the most convenient and cost effective in our review.

Discussion and results of the protection circuit operation are presented. Usefulness of such a circuit in connection with a PWM motor drive was demonstrated. The results showed that even the most efficient IGBT's with the worst short-circuit capability can be protected effectively without detrimentally affecting the normal system operation.

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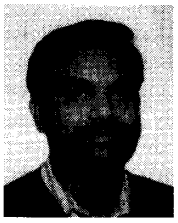

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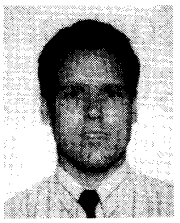

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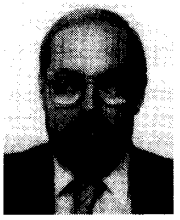

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